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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,560	12/31/2003	David W. Boggs	111079-135918	5692

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EXAMINER	
PATEL, ISHWARBHAI B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,560	BOGGS ET AL.	
	Examiner	Art Unit	
	Ishwar (I. B.) Patel	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *9-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 19-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 19-23 are objected to because of the following informalities: Regarding claim 19, the phrase "an electronic substrate interconnected with.....", line 3, and "a substrate including ....., line 5, are misguiding. For the examination purpose, both "an electronic substrate" and "a substrate" are considered as the same substrate. Prior art applied accordingly.

Claims 20-23 depend upon claim 19 and inherit the same deficiency.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by anticipated

Regarding claim 1, Watanabe, in figure 13, discloses an electronic substrate comprising: a substrate (printed circuit board 21 with laminate 22) having one

electrically conductive inner layer (26); and one cavity (cavity for via 27) extending into, but not through, the substrate, exposing one electrically conductive inner layer (26).

Regarding claim 2, Watanabe further discloses one electrically conductive surface Layer (24), wherein the interconnect cavity extends from the electrically conductive surface layer (24) to the electrically conductive inner layer (26).

Regarding claim 3, Watanabe further discloses the interconnect cavity comprises a base (base of the cavity for via 27) adjacent to the electrically conductive inner layer (26), the base comprising a layer of electrically conductive material (10, 27b).

Regarding claim 4, Watanabe further discloses the interconnect cavity comprises a base (base of the cavity for via 27) adjacent to the electrically conductive inner layer (26), wherein the interconnect cavity defines a wall (wall of the cavity for via 27) interconnected with the base adjacent electrically conductive inner layer (26).

Regarding claim 5, Watanabe further discloses the interconnect cavity comprises a base (base of the cavity for via 27) adjacent to and electrically interconnected with the conductive inner Layer (26), the interconnect cavity extending from a surface layer (24) defines a wall (wall of the cavity for via 27) interconnected with the base adjacent electrically conductive inner layer (26) and the surface layer (26).

Regarding claim 6, Watanabe further discloses the interconnect cavities is adapted to receive and interconnect with electrically conductive interconnect material (the cavity is receiving the conductive layer, 8, 27a,b and 11).

4. Claims 1-8 and 19-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Ho et al., US Patent No. 6,717,264.

Regarding claim 1, Ho et al., in figure 4F, discloses an electronic substrate comprising: a substrate (substrate 100, column 6, line 21, made up of dielectric layer 120 and 125) having one electrically conductive inner layer (130); and one cavity (cavity of via 260, shown in detail in figure 2 as reference element 110) extending into, but not through, the substrate, exposing one electrically conductive inner layer (130).

Regarding claim 2, Ho et al., further discloses one electrically conductive surface layer (200), wherein the interconnect cavity extends from the electrically conductive surface layer (200) to the electrically conductive inner layer (130).

Regarding claim 3, Ho et al., further discloses the interconnect cavity comprises a base (base of the cavity for via 260) adjacent to the electrically conductive inner layer (130), the base comprising a layer of electrically conductive material (200).

Regarding claim 4, Ho et al., further discloses the interconnect cavity comprises a base (base of the cavity for via 260) adjacent to the electrically conductive inner layer (130), wherein the interconnect cavity defines a wall (wall of the cavity for via 260) interconnected with the base adjacent electrically conductive inner layer (130).

Regarding claim 5, Ho et al., further discloses the interconnect cavity comprises a base (base of the cavity for via 260) adjacent to and electrically interconnected with the conductive inner layer (130), the interconnect cavity extending from a surface layer (200) defines a wall (wall of the cavity for via 260) interconnected with the base adjacent electrically conductive inner layer (130) and the surface layer (200).

Regarding claim 6, Ho et al., further discloses the interconnect cavity is adapted to receive and interconnect with electrically conductive interconnect material (see figure 4F).

Regarding claim 7, Ho et al., further discloses the interconnect cavities are positioned to correspond with land pads (310) of a surface mount technology electrical component (300).

Regarding claim 8, Ho et al., further discloses at least one of

the interconnect cavities comprises a base (base of the cavity for via 260) adjacent to the electrically conductive inner Layer (130) and an opening at a surface of the substrate, the base having a smaller diameter than the opening (see figure 4F).

Regarding claim 19, Ho et al., in figure 4F, discloses an electronic device comprising: an electronic component (300) having component interconnects (320), and an electronic substrate with at least one of electronic component having: a substrate (substrate 100, column 6, line 21, made up of dielectric layer 120 and 125) including one electrically conductive inner layers (130); and one or more interconnect cavities (cavity of via 260, shown in detail in figure 2 as reference element 110) extending into a surface of, but no through the substrate exposing one electrically conductive inner layer (130).

Regarding claim 20, Ho et al., further discloses the substrate further comprises one electrically conductive surface Layer (200), wherein one or more of the interconnect cavities extends from at least one of the surface Layer (200) to the electrically conductive inner layer (130).

Regarding claim 21, Ho et al., further discloses at least one of the interconnect cavities comprises a base (base of the cavity for via 260) adjacent to the electrically conductive inner layer (130), the base comprising a layer of electrically conductive material (200).

Regarding claim 22, Ho et al., further discloses at least one of the interconnect cavities comprises a base (base of the cavity for via 260) adjacent to the electrically conductive inner layer (130), wherein the interconnect cavity defines a wall (wall of the cavity for via 260) interconnected with the base adjacent conductive inner layer (130).

Regarding claim 23, Ho et al., further discloses the electronic component is a microelectronic die (chip 300).

Response to Arguments

5. Applicant's arguments with respect to claims 1-8 and 19-23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Akram, US Patent No. 6,127,736, in figure 4, discloses cavities connected with inner layer having interconnection material in the cavities and a die (38) mounted on the substrate.

Scholz, US Patent No. 5,329,423, in the embodiment of figure 1, discloses an interconnect structure with interconnect material (bump 24) formed on the component

and in the embodiment of figure 3, an interconnect structure with interconnect material (bumps 58,60) formed on the substrate.

Akram, US Patent No. 6,646,286, in figure 26, discloses interconnection structure with a die (186) having interconnect material (180) connected to a substrate having cavity.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IBP
Ishwar (I. B.) Patel
Examiner
Art Unit: 2841
July 29, 2005

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